Clean copy of the amended claims

1. A method for generating operationally limited hardware and software for a programmable device, the method comprising:

identifying license information associated with a protected intellectual property block configured for implementation on the programmable device, wherein the license information identifies a parameter associated with a prototype operation range and a production operation range; and

generating operationally limited hardware and software, wherein the hardware and software are operationally limited using the parameter identified in the license information associated with the intellectual property block.

2. (Canceled).

3. The method of Claim 2 wherein the parameter is a hardware parameter.

4. The method of Claim 3 wherein the hardware parameter is a data format.

5. The method of Claim 3 wherein the hardware parameter is a number of pin contacts between the hardware and an external device.

6. The method of Claim 3 wherein the hardware parameter is a signal limit.

7. The method of Claim 6 wherein the signal limit is a limit on a number of input signals allowed into the hardware by the software.

8. The method of Claim 6 wherein the signal limit is a limit on a number of output signals allowed out of the hardware by the software.

9. The method of Claim 8 wherein the output signals are signals used to provide a status of either the hardware or the software.

10. The method of Claim 3 wherein the parameter is set by preselected fabrication of the hardware.

11. The method of Claim 3 wherein the parameter is set by preselected augmentation of the hardware.

12. The method of Claim 2 wherein the parameter is a software parameter.

13. The method of Claim 12 wherein the parameter is a time limit on run time during which the software will permit operation of the hardware.

14. The method of Claim 61 further comprising disabling the hardware after the run time has reached the time limit.

15. The method of Claim 14 wherein disabling the hardware comprises a reset of a register in the hardware.

16. The method of Claim 14 wherein disabling the hardware comprises a global tri-state of hardware IO.

17. The method of Claim 14 wherein disabling the hardware comprises a random failure of the hardware.

18. The method of Claim 14 wherein an internal clock of the hardware is used to measure the run time of the hardware.

19. (Canceled).

20. (Canceled).

21. (Canceled).

22. A method for disabling a hardware during operation of the hardware, wherein the hardware is a programmable chip configured using a software tool having access to a plurality of intellectual property blocks for implementation on the programmable chip, the method comprising:

identifying a run time limit that is (i) long enough to permit testing of the hardware in a prototype operation mode and (ii) too short for use of the hardware in a production operation mode, wherein the run time limit has been set using license information associated with at least one of the plurality of intellectual property blocks;

measuring a time elapsed during operation of the hardware; and

disabling the hardware after the time elapsed reaches the run time limit.

23. The method of Claim 22 wherein measuring the time elapsed is performed using an internal clock associated with the hardware.

24. The method of Claim 22 wherein disabling the hardware comprises a reset of a register in the hardware.

25. The method of Claim 22 wherein disabling the hardware comprises a global tri-state of hardware I/O.

26. The method of Claim 22 wherein disabling the hardware comprises a random failure of the hardware.

27. (Canceled).

28. (Canceled).

29. (Canceled).

30. A programmable chip that can be operationally limited during operation, comprising:

a clock operable to measure a run time;

a memory including a run time limit, the run time limit being (i) long enough to permit testing of the programmable chip in a prototype operation mode and (ii) too short for use of the programmable chip in a production operation mode, wherein the run time limit has been selected at least in part using license information associated with a protected intellectual property block; and

circuitry configured to disable the programmable chip after clock measures that the run time has reached the run time limit.

31. The programmable chip of Claim 30 wherein the programmable chip is disabled using one of the following:

a reset of a register in the programmable chip,

a global tri-state of I/O of the programmable chip, and

a random failure within the programmable chip.

32. (Canceled).

33. (Canceled).

34. A computer program product associated with a computer readable medium including computer code which when executed on a computer performs a process of generating operationally limited hardware and software for a programmable chip, the computer program product comprising:

computer code for identifying a protected intellectual property block associated with a design for implementation on the programmable chip;

computer code for identifying a parameter using license information associated with the protected intellectual property block, wherein the parameter is associated with a first operation range and a second operation range; and

computer code for generating operationally limited hardware and software, wherein the hardware and software are operationally limited based on the parameter identified using license information.

35. The computer program product of Claim 34 wherein the parameter is a hardware parameter.

36. The computer program product of Claim 35 wherein the hardware parameter is a data format.

37. The computer program product of Claim 35 wherein the hardware parameter is a number of pin contacts between the hardware and an external device.

38. The computer program product of Claim 35 wherein the hardware parameter is a signal limit.

39. The computer program product of Claim 38 wherein the signal limit is a limit on a number of input signals allowed into the hardware by the software.

40. The computer program product of Claim 38 wherein the signal limit is a limit on a number of output signals allowed out of the hardware by the software.

41. The computer program product of Claim 40 wherein the output signals are signals used to provide a status of either the hardware or the software.

42. The computer program product of Claim 35 wherein the parameter is set by preselected fabrication of the hardware.

43. The computer program product of Claim 35 wherein the parameter is set by preselected augmentation of the hardware.

44. The computer program product of Claim 34 .wherein the parameter is a software parameter.

45. The computer program product of Claim 44 wherein the parameter is a time limit on run time during which the software will permit operation of the hardware.

46. The computer program product of Claim 45 further comprising computer code generating operationally limited hardware and software for disabling the hardware after the run time has reached the run time limit.

47. The computer program product of Claim 46 wherein disabling the hardware comprises a reset of a register in the hardware.

48. The computer program product of Claim 46 wherein disabling the hardware comprises a global tri-state of hardware IO.

49. The computer program product of Claim 46 wherein disabling the hardware comprises a random failure of the hardware.

50. The computer program product of Claim 46 wherein an internal clock of the hardware is used to measure the run time of the hardware.

51. (Canceled).

52. (Canceled).

53. (Canceled).

54. A system for generating operationally limited hardware and software for a programmable chip, the system comprising:

means for identifying a protected intellectual property block associated with a design for implementation on the programmable chip;

means for identifying license information associated with the protected intellectual property block, wherein the license information identifies a parameter associated with a first operation range and a second operation range; and

means for generating operationally limited hardware and software, wherein the hardware and software are operationally limited using the parameter identified in the license information.

55. (Canceled).

56. (Canceled).

57. The system of Claim 54 wherein the operational parameter is time and further wherein the first operation range is a prototype operation time range and the second operation range is a production operation time range.

58. The system of Claim 57 wherein the prototype operation time range has a maximum and further wherein the production operation time range has no maximum.

59. The system of Claim 54 wherein the first operation range is a range of timed operation having a maximum time limit and wherein the second operation range is a range of timed operation extending beyond the maximum time limit.

60. (Canceled).

61. The method of claim 1 further comprising:

operating the hardware and the software in a prototype operation mode and in a production operation mode;

operationally limiting the hardware and the software in the prototype operation mode.